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Protection of Transmission Lines with Series Compensation
New Tools

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1 INTRODUCTION

Properly protecting a transmission line of extra high voltage equipped with series compensation it is still a major challenge for the system protection engineers. The applied conditions resulting from this configuration still present operating conditions not properly resolved that entail great difficulties in determining your settings, and with the risk of an almost certain improper actuation eminent for the reasons to be exposed during the presentation of this work. Another aspect to be considered is that, in many of these applications, the manufacturers of relays available in the market today present the characteristic impedance type MHO or quadrilateral for measurement of these impedances, which implies in some cases to increase the performance of the respective protection zones (mostly the zone 1), compromising their respective times of network stability or reducing significantly your range precisely because of the presence of these capacitors looking to avoid undue performances for faults in parallel circuits and or at the beginning of the circuit.

The present work had, as a main motivation, the results obtained during the tests performed by the company *Farfilho Consulting Trading and Representations LTDA*, hired by IENE, for the coordination and execution of the tests for protection of your 500 kV lines along the RTDS (Real Time Digital Simulator) of FURNAS in 2011. These tests were designed to validate dynamically the adjustments of the protection circuit that interconnects the electric substations Colinas - São João do Piauí as shown in the diagram of the *Figure 1*.

These tests were performed in more than 600 simulations covering all types of fault scenarios in relation to the specific protection to the spark-gaps of banks and whether these systems work or not. The most important conclusion of these tests is that they reduce the range of Zone 1 (around 50%) of the line terminals, due to the overreach of same for external faults in parallel line due to the presence of sub synchronous component *(Tables 1 and 2)*, which made the system protection of these lines virtually dependent only on the adjustments of the zone 2, associated with the system of teleprotection scheme POTT (Permissive Overreaching Transfer-Trip).

In possession of the arguments cited, this work will propose steps to minimizing these operating conditions developed for operation in parallel with the Fourier algorithm common to all manufacturers of digital signal processing techniques, such as the Wavelet Transform [4.3, 4.5], concepts of pattern recognition through analysis of the clusters, and finally of the neural networks to detect the presence or absence of a series capacitor in the fault loop. These conditions detected should occur in a time less than or equal to 1 cycle, and once detected the series capacitor in this loop will be used as the principle of traveling waves (ΔI, ΔV) [4.4] to be able to see the fault with the correct directionality and with the maximum possible range of the protected line. These procedures will increase the reliability and make redundant the currently operating protections in the system with zone 2 added to the relay protection system POTT (Permissive Overreaching Transfer-Trip) [4.1]. Then, these algorithms will be tested on 500 kV circuit presented in *Figure 15*.

2 - Objective

2.1 Theoretical Concepts

The two most important operating conditions as a result of this application on the agenda are as follows:

- Current reversal: this condition, presented in *Figure 2*, occurs when *Equation [1]* is true
- Voltage reversal: this condition, presented in *Figure 3*, occurs when *Equation [2]* is true

In some ways, the conditions presented above can be avoided belong the project and the definition of the level of compensation to be effected in the line, together with the equivalent network and other system informations. The component sub synchronous already present in the current waveforms depends on whether the series capacitor is inserted, or not, in the fault loop. Here is made a brief analysis of a single-phase R-L-C circuit for the two main conditions where the solution of differential equations of R-L (Inductive Loop) and R-L-C circuit (Inductive and Capacitive Loop) have the following main characteristics:

- <u>RL Circuit:</u> DC Component and fundamental frequency of 60 Hz
- <u>RLC Circuit:</u> DC Component, fundamental frequency of 60 Hz and natural frequencies damped oscillatory frequencies

These natural frequencies ω_d are obtained from the roots of the complex differential equation and display the values given by *Equation [3]*.

In the *Figures 4 and 5* are presented both typical waveforms through the modeling of a single-phase circuit in ATP software.

These concepts can be extended to transmission systems, where the lines with distributed parameters modeled by compensation factor that adds to the aspects cited the high-frequency components present in current waveforms, due to reflections of waves that travel to the condition of faults on the line with the presence or absence of these banks. Another important aspect to be seen is the operating excursion impedance vector for the condition of the inductive - capacitive loop. From the modelling performed in MATLAB with typical Fourier algorithms for extraction of the modules and phase of the voltage and current vectors, where we can observe the excursion of the vector impedance for a typical three-phase fault. Unlike the inductive loop featuring a characteristic more well behaved in R-X, that have an oscillatory behavior due to the presence of ω_d frequency, showing a form similar to a logarithmic spiral. This characteristic is responsible for possible underreach or overreach in these protection relays, as shown in *Figure 6*.

2.1.1 Development of Algorithms

2.1.1.1 Algorithm Classification

To clarify, the main problem so far for this type of application is the presence of series capacitors in the fault loop. The intention here is to propose a digital algorithm, operating in parallel with the conventional impedance measurement that detects the presence or not of a capacitor on this loop. Once detected, the same protection system uses the discrimination of directionality concepts of ΔV and ΔI by wave travelling [4.1,4.4], blocking the action of Zone 1 for these conditions. By the concepts already presented this shows that the problem is typically classification, i.e., identify if the fault loop is inductive or capacitive-inductive. The primary tool to be used in the classification will be the Wavelet Transform which is well known in the academic world and widely used [4.3,4.5], where the main objective is to detect the high frequencies to be captured in the current signals. In summary, this transformed form multiplies the input discrete signal by a series of functions well behaved at the time called Wavelet Mother. These do nothing more than answer the urge to filters high - pass and low - pass. Then, after this multiplication, moved this signal by 2, and so on, increasing the resolution in frequency at the expense of reply in time.

These multiplications results in levels with their Wavelet coefficients (Details (D) and approach (A)) indicating the presence of this frequency in the range under analysis. The main difference of this tool, compared to the Fourier transform, is the fact of owning an Escalation Parameter (a) shown in *Equation [4]*, which enables a logarithmic scale for the analysis of the sign in question. This is unlike the Fourier Transform that defines the size of the watch window and displays the same resolution for the entire frequency spectrum of the signal.

In *Figure 7* is presented the block diagram of the algorithm MRA (Multi Resolution Analysis) used for Wavelets analysis.

For the first tests using the above tool modelled on the ATP circuit R-L-C with concentrated parameters using the values obtained from the circuit of *Figure 1* and shown some of the values used in *Table 3* below. In *Table 4* then the Wavelet decompositions are presented and the amount of samples contained in windows, 1/2, 3/4 and 1 cycle of 60 Hz was used for the development of the algorithm in a sampling frequency of 512 samples/cycle or 30720 Hz, which provides measurements of the frequency bands listed in its decomposition levels as shown in the diagram of *Figure 7*.

From here on this kind of algorithm is modeled on ATP a 500 kV double circuit, generating 70 cases in total, being 30 cases to the inductive loop and 40 cases for the inductive-capacitive loop, varying the angles of fault incidence (0 and 90 degrees), the level of compensation of the lines (50 and 70%) and the source impedances, reproducing within the possible operating conditions found in tests performed in FURNAS[4.6].

2.1.2.2 The Neural Network and the Clustering Analysis

The window size and the wavelet level used to detect the presence of a series capacitor was chosen through a bi-dimensional cluster analysis of wavelet coefficient presented in *Figure 10* and to neural network training and testing the data were separated into two sets, where the first strategy was to pick up differences in the high frequencies of the signal due to the presence or not of the capacitor through the wavelet detail levels.

It can be seen by the results obtained that the data is not overlapping; however there is a linear separation, not getting a proper classification. The second strategy is to get the fastest current decay due to the presence of sub-synchronous frequency in the inductive-capacitive signal. To this end, it was used the 8 level approximation component of wavelet transform with the goal of obtaining a filtered signal eliminating the highest frequencies that could interfere with the measurement in this decay. To measure the speed of the decay it was used an approximation of the derivative through the differences between consecutive samples. In the *Figure 11* is shown the cluster analysis based on derived vector module 8 level of Wavelet approximation using Daubechies Wavelet Mother 10 and using a data window of 3/4 of a cycle.

Therefore, in general, the algorithm developed has the following steps:

→ To start the algorithm it was elaborated a criterion of overcurrent that could ensure that the data window was effectively within the fault. With the separation of this window it is calculated the coefficients of the discrete wavelet transform.

→ For the RNA training it was generated two data sets and a network test by varying the angle of incidence of the fault, the level of compensation and the fault of impedance, totaling 36 cases. The circuit used to generate this data was the circuit of *Figure 16* to enable greater ease of variation of the parameters but consistently in order to extract the characteristics of the phenomenon in question.

→ Before submitting the data to the Neural Network, these data above was normalized for better performance of the RNA training algorithm, where the form of normalization chosen was the Division of the data by the absolute maximum value in the table, using the supervised training algorithm of Resilient back propagation type which is based on the original back propagation algorithm. The above only uses the signal to determine the gradient direction to update the weights, resulting in a greater speed in overcoming the local minima of the learning curve where the gradient module approaches zero.

For this condition the RNA showed better performance when had the setting 3-30-1, and the chosen functions for activation of the hidden layer neurons and output layer were hyperbolic tangent and logistic sigmoid function respectively. As a result, the training had an error equal to 10-3 hit in 18 seasons. In the *Figures 12 and 13* are presented the basic structure of the network used and the error curve obtained for the simulated cases.

2.1.2.3 The Directionality Algorithm

Once the presence of series capacitor has been defined in the fault loop, is possible now, block the unit of Impedance on distance protection Zone 1 and use the concepts of Travelling Waves already quite well known, and used on a large scale by some suppliers. In summary, this concept based on superposition theorem uses current and voltage variations that occur in a fault window to generate the signals of ΔI and ΔV due to these variations *(Figure 15)*. These components containing all frequencies contained the signs unless the fundamental component of 60 Hz is literally the first effective incidence of waveforms, regardless of the presence or not of the capacitors in the circuit, as well as the performance of their respective protections. [4.1, 4.4].

This directionality is intrinsic to the phenomenon shown in *Figure 18* where we have polarities with different signs for faults in one direction (forward), and equal polarities in the opposite direction (backward). Another important detail that must be emphasized is their speed in detecting this directionality, i.e. around 4 ms or 1/4 of cycle.

2.1.3 Modeling and Testing

For the modeling and testing of the proposed algorithm, it was made up the 500 kV circuit in MATLAB/Simulink software as shown on diagram of *Figure 19*. The measurement terminal was placed in each terminal and these measurements should be considered important with regards the above. The capacitor Series have two Bank's own intrinsic protections that are quick acting (performance ≤ 1ms) and slow acting (≤ 25ms). For the project, will be consider that having internal faults on the line and when there is action of the quick protections it will be considered as an inductive loop, and for slow protections, as inductive-capacitive loop.

Therefore, in this circuit 10 cases with incidence angle of 0° and 90° on the distances of 25,50 and 75% of the terminal for internal two Phase faults. Then they were generated 04 cases in parallel line to 50 and 75% with the same types of faults. By the characteristics adjusted for the intrinsic protections of banks had for these conditions 03 cases of fast acting protection (RL circuit) and 07 cases of slow protection performance (RLC circuit). The cases of fast acting protections were mainly the DC component of the fault current to shift the same in the time axis. In the *Figure 19* are presented the performances of currents and voltages of the MOV bank as well as the typical voltages and current forms obtained in these simulations as a typical curve MHO to one of simulated cases.

2.2 - Equations

[1] $|Xc| > |XF + XL|$
[2] $|Xc| < |XF + XL|$ and $|Xc| > |XL|$

[3] $$\omega_d = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

[4] $$(W_\psi x)(m,n) = \frac{1}{\sqrt{a0^m}} \int_{-\infty}^{+\infty} x(t).\psi\left(\frac{t - n.a0^m \cdot b0}{a0^m}\right).dt$$

Where:
a → Parameter scale
b → Translational Parameter with m and n and Z, a0 > 1 and b0 # 0

2.3 - Figures and Tables

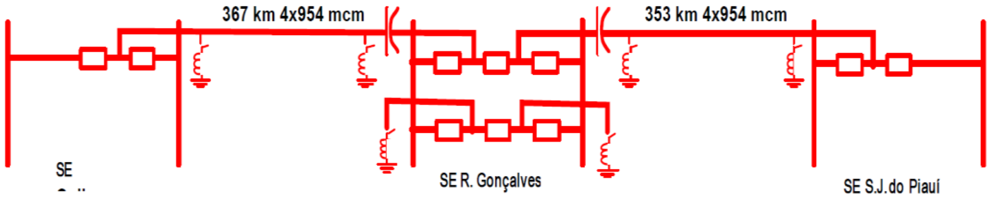

Figure 1: 500 kV System – IENE – SE's Colinas – Ribeiro Gonçalves – São João do Piauí
Note: All reactors are banks of 3x60 Mvar
Capacitive compensation series of 48% in LT COL-RGO and 49% in LT RGO-SJP

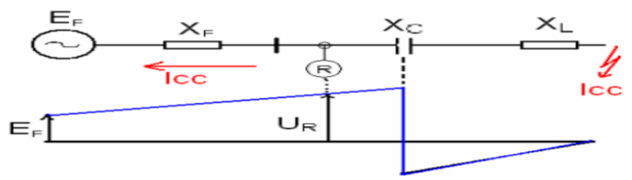

Figure 2: Current Reversal

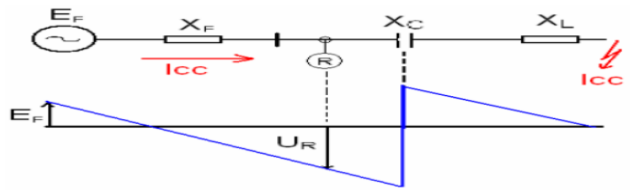

Figure 3: Voltage Reversal

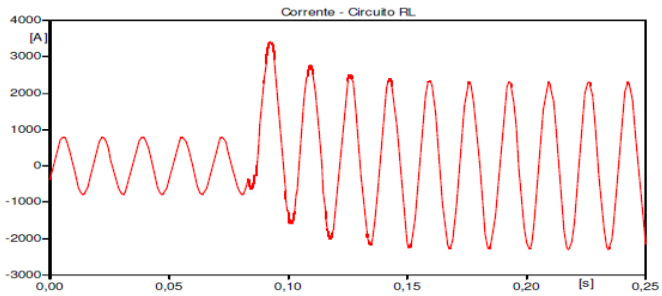

Figure 4: Typical Current Waveform - RL Circuit

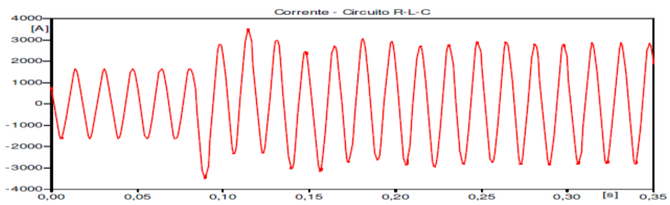

Figure 5: Typical Current Waveform - RLC Circuit

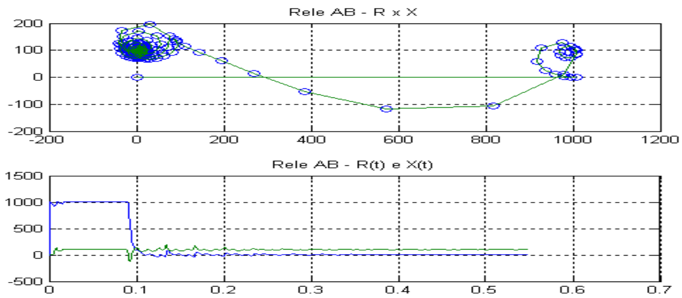

Figure 6: Excursion of Impedance Vector - Inductive/Capacitive Loop

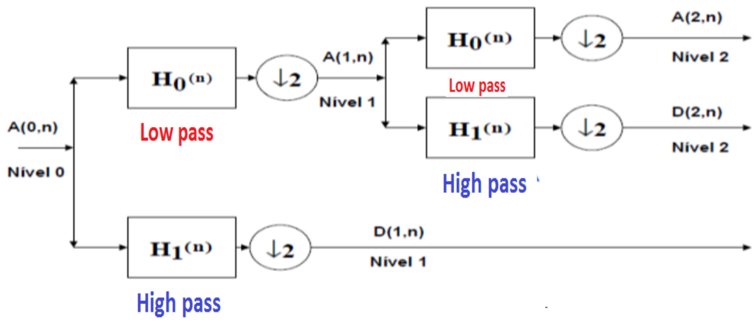

Figure 7: MRA Algorithm - Multi Resolution Analysis

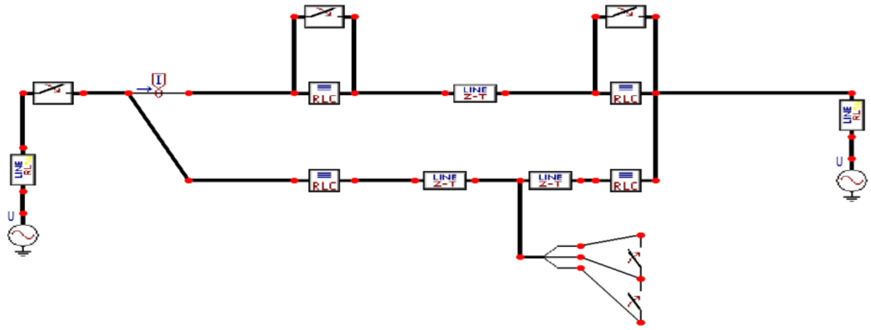

Figure 8: Circuit Modelled in ATP platform

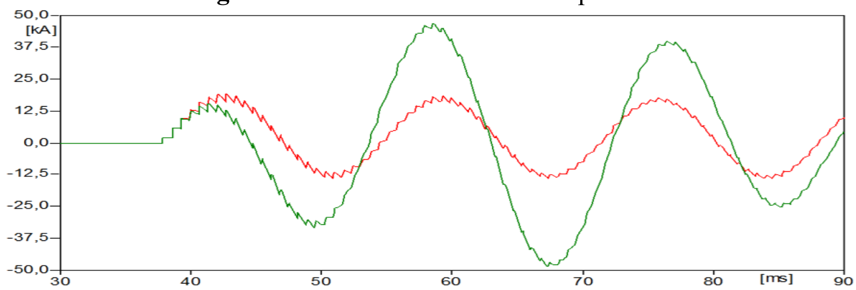

Figure 9: Typical waveforms for fault Loops
Red → Inductive Loop
Green → Induction/Capacitive Loop

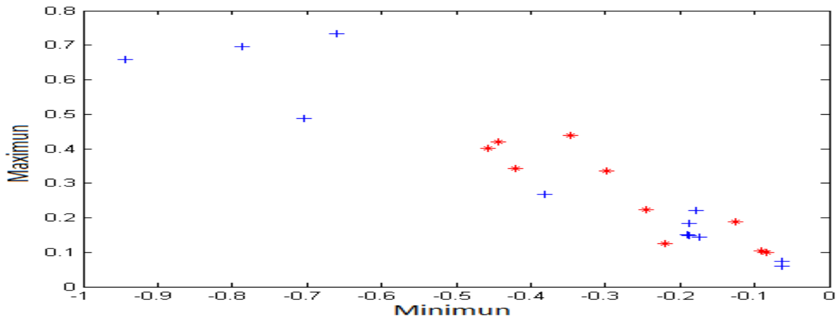

Figure 10: Cluster analysis - Level 5 (Wavelet Detail)

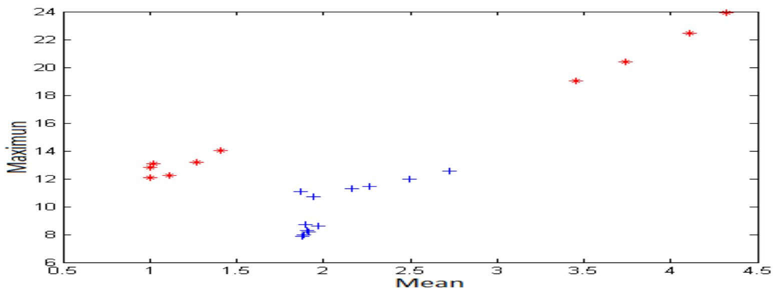

Figure 11: Cluster analysis - derived from Wavelet approximation of level 8

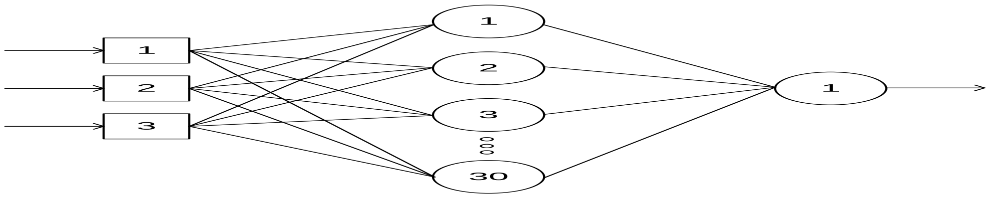

Figure 12: Artificial Neural network

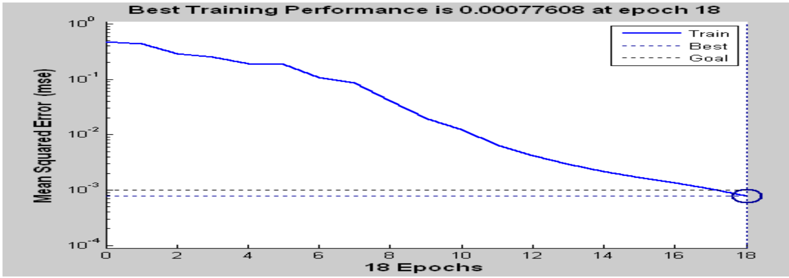

Figure 13: Error Graphic

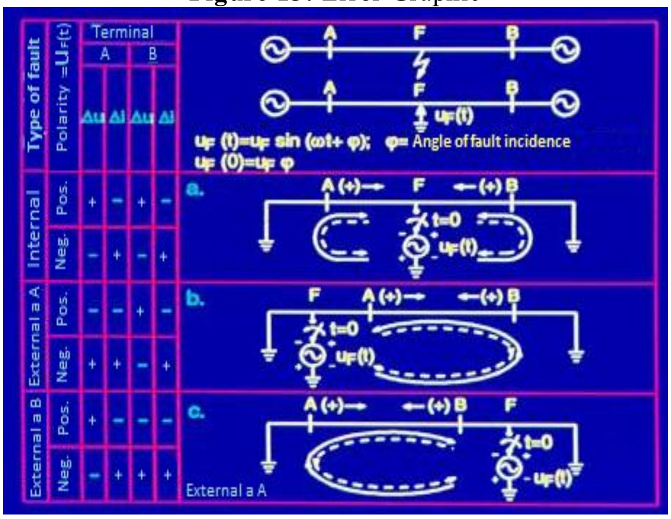

Figure 14: Polarity and ΔI and ΔV polarization

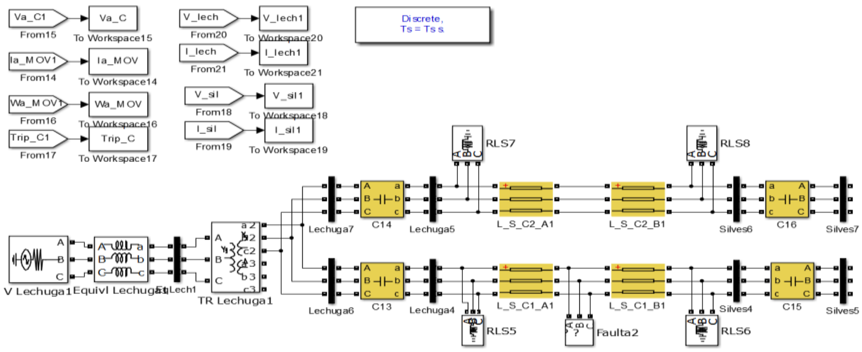

Figure 15: 500 kV diagram for final tests - MATLAB/Simulink Platform

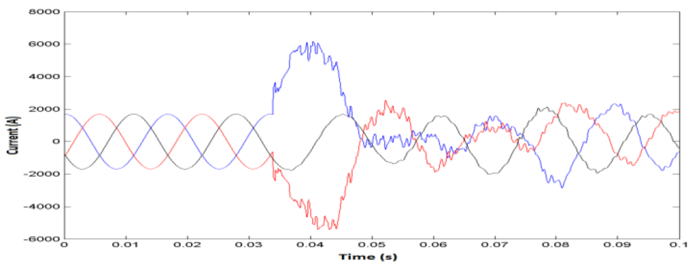

Figure 16: Current Waveforms

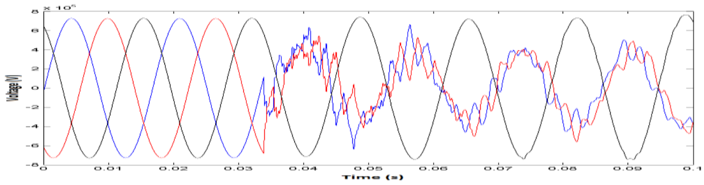

Figure 17: Voltage Waveforms

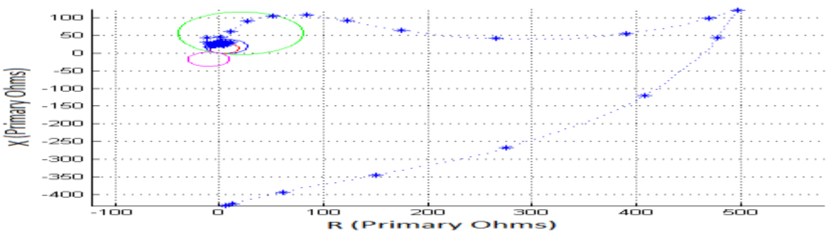

Figure 18: Impedance Diagram

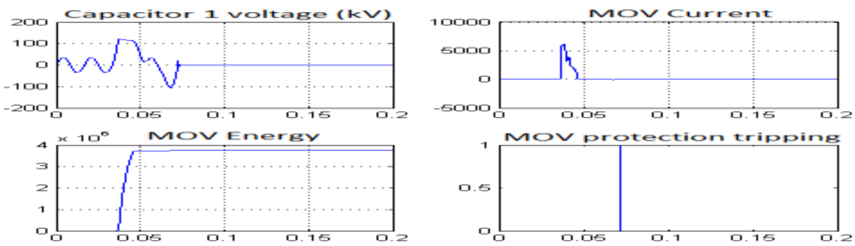

Figure 19: Curves of voltages, currentes and MOV in the capacitor

	Initial Value		Final Value	
	Z1P	Z1N	Z1P	Z1N
Ribeiro Gonçalves	30.67 Ω	26.22 Ω	15.94 Ω	13.11 Ω
São João do Piauí	2.49 Ω	2.22 Ω	2.24 Ω	1.99 Ω

Table 1: Changing settings of the 500 kV line - Ribeiro Gonçalves - São João do Piauí

Settings	Initial Value		Final Value	
	Z1P	Z1N	Z1P	Z1N
Ribeiro Gonçalves	28 Ω	25.78 Ω	14.56 Ω	12.89 Ω
Colinas	13.40 Ω	12 Ω	11.39 Ω	9.96 Ω

Table 2: Changing settings of the 500 kV line - Ribeiro Gonçalves – Colinas

Source (V)	CS (Hz)	Resistance (Ω)	Indutance (Ω)	Capacitance (Ω)	Indutance (mH)	Capacitance (µF)
408248.29	3 Hz	7.106	100.6	0.2515	266.843	10546.79
408248.29	10 Hz	7.106	100.6	2.79	266.843	9507.23

408248.29	58 Hz	7.106	100.6	94	266.843	28.21
408248.29	60 Hz	7.106	100.6	100.6	266.843	26.36

Table 3: Parameters of the R-L-C Circuit for Wavelet analysis

Frequency (Hz)	Level	Window of ½ cycle	Window of ¾ cycle	Window of 1 cycle
15360 - 7680	1	128	170	256
7680 - 3840	2	64	85	128
3840 - 1920	3	32	42	64
1920 - 960	4	16	21	32
960 - 480	5	08	10	16
480 - 240	6	04	05	08
240 - 120	7	02	03	04
120 - 60	8	01	01	02
60 - 30	9	-	-	01

Table 4: Wavelet Frequencies Decomposition(Samples)

3 - CONCLUSION

The results obtained are encouraging with respect to the search for an alternative application for the protection of lines with series compensation. Digital signal processing and pattern recognition new techniques are presented as a good way for solving system protection problems that are still not properly solved.

However, there is still a requirement for greater robustness in its algorithms so that they can become effective in the near future. In case of this developed application, the above should be tested to a larger and more comprehensive number of cases, as well as being analyzed to try to detect the presence of the sub synchronous component with the shortest possible window size.

4 - REFERENCES

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